Large Synoptic Survey Telescope

www.lsst.org

LSST Camera Electronics

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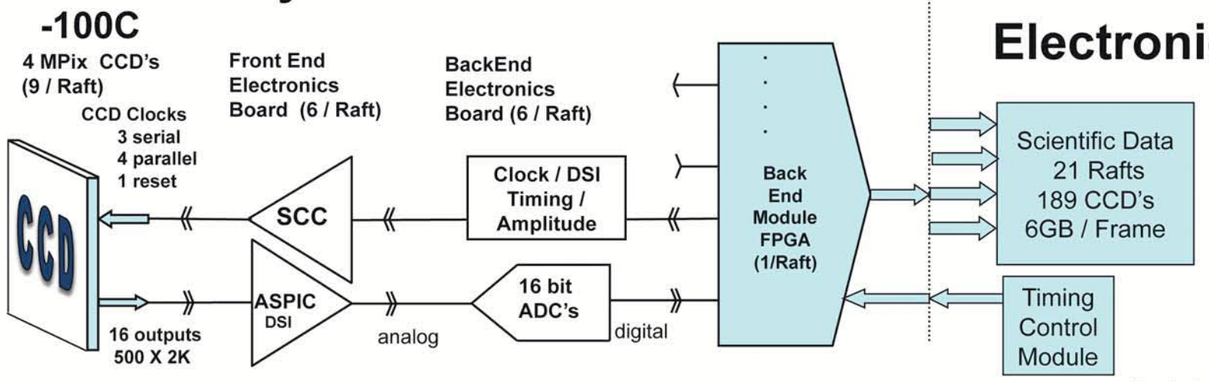
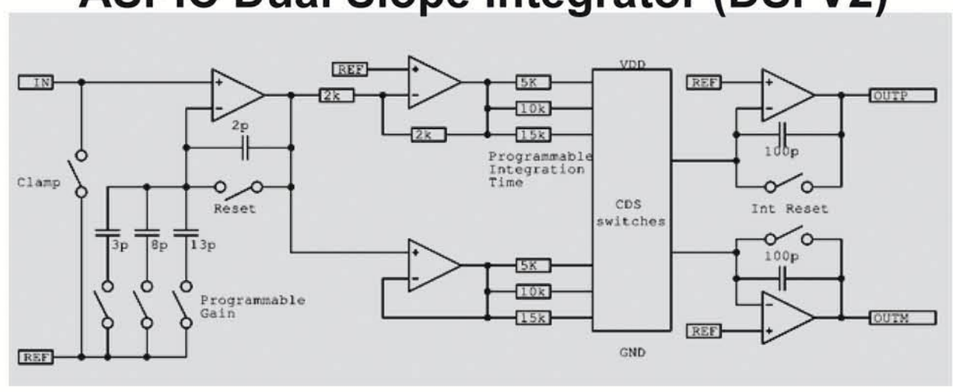
The 3.2 Gpixel LSST camera will be read out by means of 189 highly segmented 4K x 4K CCDs. A total of 3024 video channels will be processed by a modular, in-cryostat electronics package based on two custom multichannel analog ASIC's now in development. Performance goals of 5 electrons noise, .01% electronic crosstalk, and 80 mW power dissipation per channel are targeted. The focal plane is organized as a set of 12K x 12K sub-mosaics ("rafts") with front end electronics housed in an enclosure falling within the footprint of the CCDs making up the raft. CCD surfaces within a raft are required to be coplanar to within 6.5 microns. The assembly of CCDs, base-plate, electronics boards, and cooling components constitutes a self-contained and testable 144 Mpix imager ("raft tower"), and 21 identical raft towers make up the LSST science focal plane. Electronic, mechanical, and thermal prototypes are now undergoing testing and results will be presented at the meeting.

Cryostat Electronics

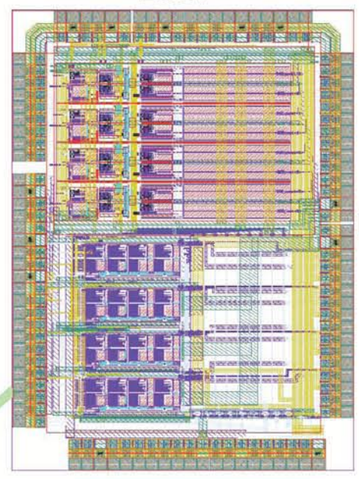


Warm Electronics

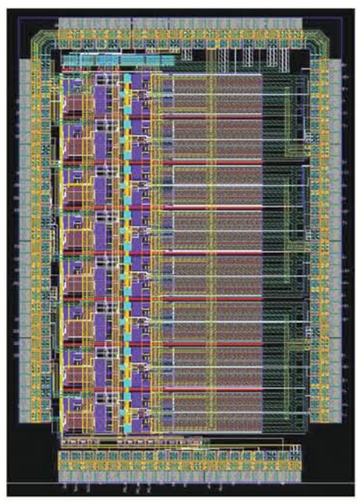
ASPIC Dual Slope Integrator (DSI V2)



Prototype CCD Readout ASPIC V1
AMS CMOS 5V .35um process
(IN2P3 France)
2007

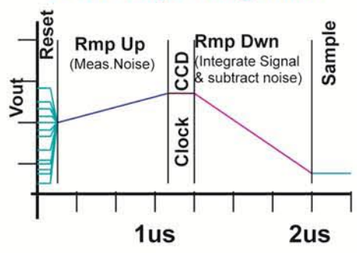


8 channel DSI CCD Readout ASPIC V2
25mW / ch
AMS CMOS 5V .35um process
2008-9

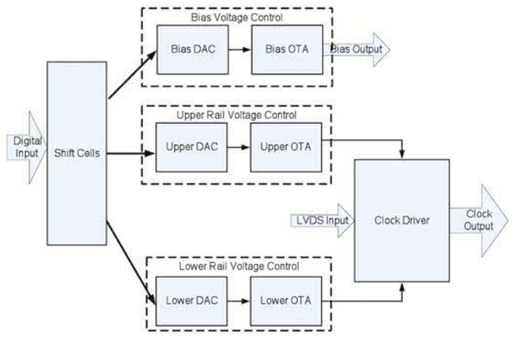


8 Dual Slope Integrators
- **~5nV / √Hz**
- **500KHz Operation**
- **.01% Crosstalk**
- **150K e Full Well capacity**
- **Differential outputs**
- **Output Drive > 50pF**
- **Supply +5V**

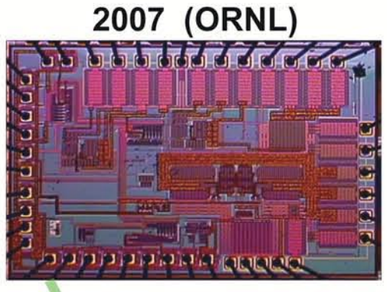
Dual Slope Integration



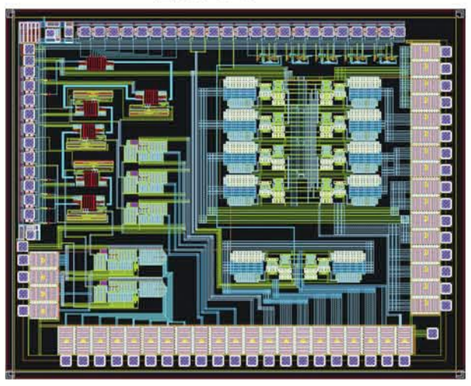
Sensor Control Chip (SCC)



Prototype SCC Sensor Control ASIC
2X3mm 1 clock, 1 bias control
2007 (ORNL)

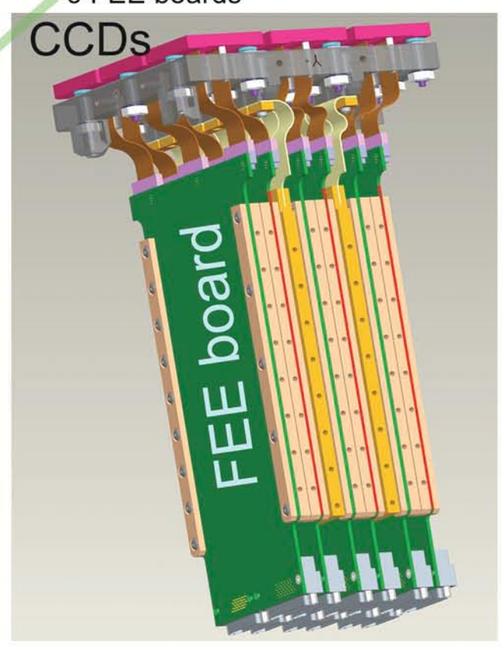


Sensor Control ASIC
5 CCD Clock channels, 13 bias lines
ATMEL SMARTIS 50V .8um process
2008-9



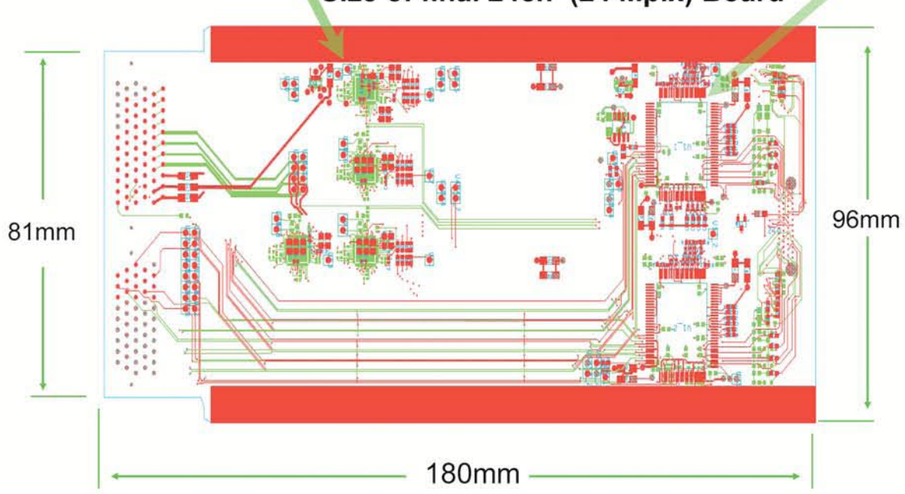
CCD Raft Module

- 9 X 16 Mpix 4X4cm CCD's
- 144 RO channels@500KHz
- 6 FEE boards



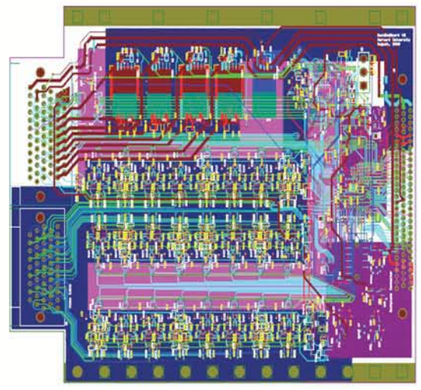
8 Channel Prototype ASIC Test PCB

December 2008
Size of final 24ch (24 Mpix) Board

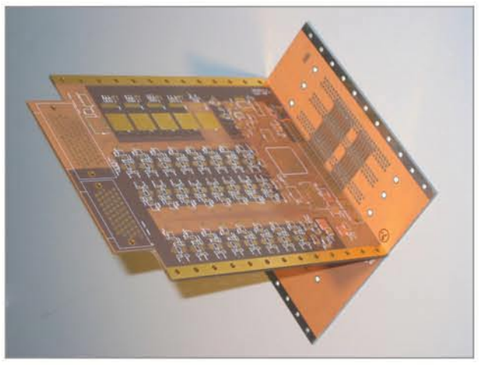


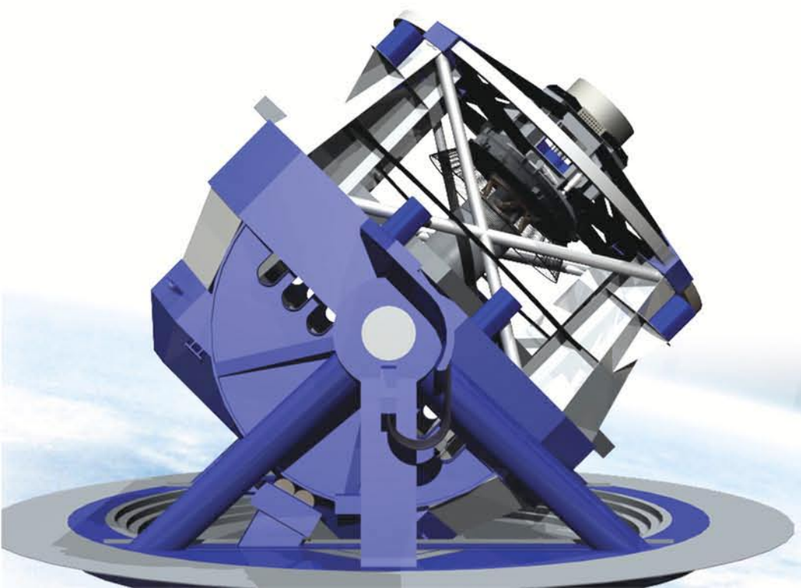
Back End Electronics (BEE) Board

DSI readout 24, 16 bit ADC's
CCD Clock timing / Amplitude control
Supply and Temp monitoring

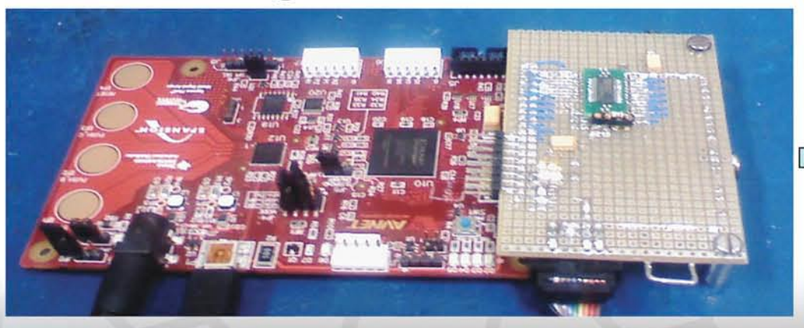


Fabricated BEE Board And Backplane





CCD Signal Emulator



500 Khz Drive

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