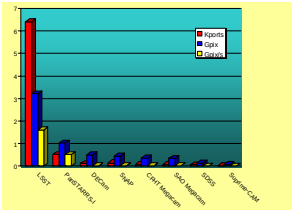
Readout Electronics for the 3.2 Gpixel LSST Focal Plane

John Oliver, Nathan Felt (Harvard),
Paul O'Connor, Veljko Radeka (BNL),
John Geary (Harvard Smithsonian, CfA)

The requirements for reading out the focal plane of the Large Synoptic Survey Telescope are driven by the scientific goals of simultaneously achieving exceptionally high throughput and faint limiting magnitude (i.e., 10 square degrees imaged to 24 AB magnitude every 15 s). This results in a large pixel count (3Gpix) and very high segmentation (6,400 readout channels) operating at modest pixel rates (250 kHz). About six gigabytes of data are generated per exposure. Present plans call for installing front end electronics (ASIC-based analog processing) inside the cryostat adjacent to the sensors at a temperature of -100C. Digitizing and multiplexing electronics will be in a separate thermal zone within the main cryostat, and data will exit the cryostat over a small number of optical fiber links. Strict attention to contamination control will be required to prevent volatile materials from the electronic hardware from condensing on the sensor surfaces. An electronics test bed is being developed at Harvard University and Brookhaven National Laboratory and the first modules will be tested in early 2006.

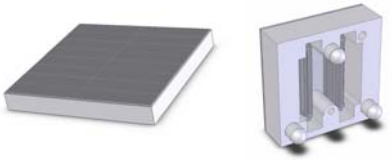
Camera Development Comparisons



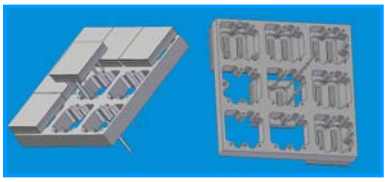
The Challenge

- ~3,200 Megapixels
- 6 e rms read noise
- 2 sec read time
- 90k e full well
- Minimize vacuum feedthrough count

32 Segment CCD imagers



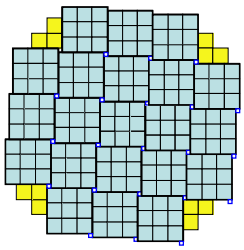
9 Sensor Raft Structure



Sensors

- 4k x 4k CCDs with 10u pixels (16 Mp)
- 10u pixels → ~ 40mm x 40mm
- Each sensor divided into 32 x 1/2MP segments (32 output ports)
- ~150 bond pads / sensor

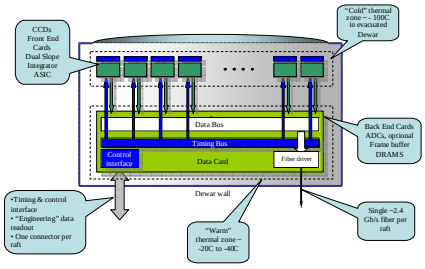
Focal Plane Array with Wavefront Sensor Locations



Rafts

- 3 x 3 array of sensors
- 288 output ports
- ~ 125mm x 125mm
- Each raft functions as an autonomous camera

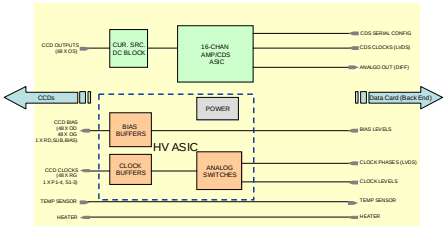
Electronics distribution in Cryostat



Focal Plane Array

- 21 fully populated rafts
- 4 partially populated "corner" rafts
- ~ 6,400 readout ports
- ~ 30,000 sensor bond pads

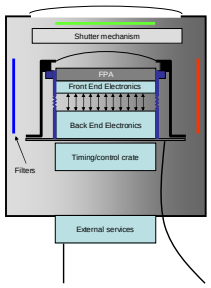
Front End ASIC Functionality



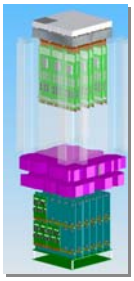
FPA Readout

- Modular by raft
- Fully synchronous
- Divided into two regions
  - ➢ Front End → Analog signal processing, clock driver translation, bias distribution
  - ➢ Back End → Analog/Digital conversion, single data fiber output
- Master "Timing & Control" card common to all rafts insures synchronicity
- FPA electronics in cryostat to minimize vacuum feedthroughs

Overall Camera Electronics Distribution



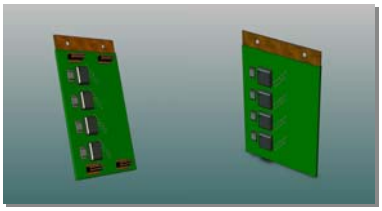
Raft Assembly with Front and Back End Electronics



Electronics packaging and cooling

- Copper core PCBs for heat conduction
- Polyimide PCBs
- Front End Electronics
  - ➢ 2x 16 Channel "Dual Slope Integrator" ASIC per sensor
  - ➢ Clock driver ASIC in HV CMOS process
- Back End Electronics
  - ➢ Octal "ADC cards" with 16 bit ADCs in 7mm x 7mm "chip scale" package
  - ➢ 40mm x ~100mm footprint
  - ➢ 4x Octal ADCs per Sensor (32 channels)

Octal ADC card (Back End)



The LSST research and development effort is funded in part by the National Science Foundation under Scientific Program Order No. 9 (AST-0551161) through Cooperative Agreement AST-0132798.
Additional funding comes from private donations, in-kind support at Department of Energy laboratories and other LSSTC Institutional Members.

National Optical Astronomy Observatory
Research Corporation
The University of Arizona
University of Washington
Brookhaven National Laboratory
Harvard-Smithsonian Center for Astrophysics
Johns Hopkins University
Las Cumbres Observatory, Inc.
Lawrence Livermore National Laboratory
Stanford Linear Accelerator Center
Stanford University
The Pennsylvania State University
University of California, Davis
University of Illinois at Urbana-Champaign