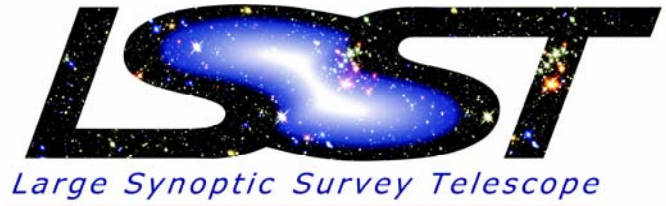


The LSST Sensor Development Program



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ABSTRACT: The LSST FPA will comprise an order of magnitude more pixels than any imaging array realized so far. The sensors must produce low read noise, high QE in the red, and a very tight PSF, which will all be necessary to do the science that LSST proposes. The principle underlying the development plan is that for an FPA involving about 200 large format sensors, an industrial approach has to be developed and adopted. In this initial phase of imager development, we will target specific technology experiments at selected vendors, with the goal of establishing both the technical characteristics of actual imagers, based on our projected imager requirements, and the industrial feasibility of their production. We have chosen to fund three projects in this initial development phase, two involving CCD technology and one utilizing hybridized CMOS architecture.

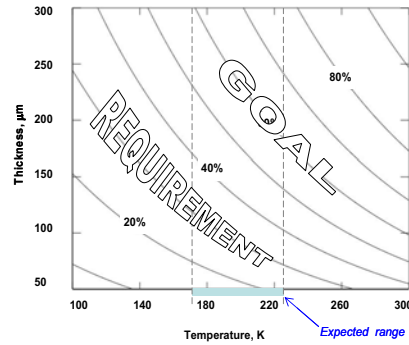
PROJECT 1

We know that the LSST imagers must have very thick high-resistivity active regions (about 100 microns thick, for high QE in the red) and be over-depleted using a backside bias voltage (for the required PSF). The two figures to the right illustrate the design tradeoffs in choosing the optimal silicon thickness for LSST.

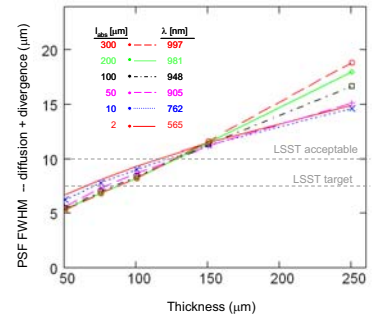
This project will involve the efforts by a major vendor of commercial CCD imagers to produce such thick, over-depleted devices, using off-the-shelf designs of established commercial production heritage on high-resistivity silicon. The deliverables to the LSST Sensor Working Group for this project are as follows:

- A. Design study for an eventual full-scale (4k X 4k format) LSST imager. Estimated delivery: March 2006
- B. Two small-format (2k X 512) CCDs of two slightly differing design on high-resistivity silicon, with required backside bias contact. Estimated delivery: July 2006
- C. One large-format (2k X 4k) CCD on high-resistivity silicon, with backside bias contact. Estimated delivery: July 2006

QE Considerations: contours of theoretical internal QE (no reflection loss) vs. sensor thickness and temperature



PSF Considerations



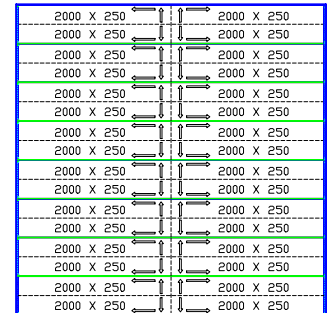
PROJECT 2

Based on experience and analysis, the LSST Sensor Working Group has established that for CCD imagers, the most desirable architecture is a highly partitioned format of 4k X 4k pixels (10-microns), with 32 output ports. An actual strawman design for such an imager has been produced and its framework drawing is presented at the right.

This project will attempt to fabricate a full-scale version of this CCD imager, on thick high-resistivity silicon and with provision for the needed backside bias contact. Because the design will necessarily be unproven in prior production, this is of course a more risky effort than the one above, but if successful, it could provide extremely valuable experimental experience before going to an actual pre-production prototype program. As partial risk mitigation, several smaller CCDs of proven design will be included on the unused chord area of the silicon wafers.

Deliverables to the LSST project are to be:

- A. First partial lot of 12 wafers, each with four large CCD imagers of slightly differing design. Estimated delivery: July 2006
- B. Last 12 wafers (production held until successful probing of the first 12). Estimated delivery: Sept. 2006
- C. First thinned device (100 microns thick): Estimated delivery: Oct. 2006



Outline of the 16 megapixel strawman CCD, showing the partitioning and charge movement for the hardwired split parallel and serial registers. All pinout for the device is along the left and right edges. The fill factor achieved in this design iteration is 96.5%.

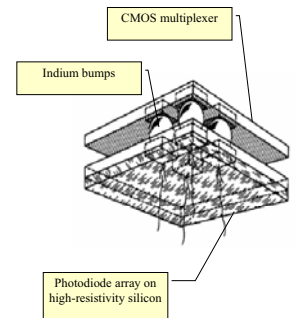
PROJECT 3

An imager based on a PIN diode array hybridized to a CMOS readout multiplexer circuit is an attractive, but largely unproven, alternative to CCD architecture. Advantages over CCD imagers include electronic shuttering, much reduced power in both the imager and support circuitry, reduced sensitivity to charge spreading from very bright stars, and non-destructive readout modes that may offer observational advantages. Disadvantages include a higher noise threshold for single reads, crosstalk between adjacent pixels and between separate outputs, and unproven ability to do precision photometry in the astronomical context.

A project to fabricate and deliver to the LSST project a complete 4k X 4k (10-micron pixel) hybridized PIN diode imager has been funded. Although the risk in such an advanced development project is large, the potential payoff in terms of a possibly superior imaging technology for LSST makes this project very attractive to us.

Deliverables to the LSST project :

- A. Device interface manual (preliminary): March 2006
- B. Operational 4k x 4k hybridized imager: Sept. 2006



Hybrid PIN-CMOS

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